APPARATUS SUITABLE FOR PROVIDING SYNCHRONIZED CLOCK SIGNALS TO A MICROELECTRONIC DEVICE

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Cross Reference to Related Applications

This application claims priority to United States Provisional Application Serial Number 60/178,373, filed January 27, 2000, entitled "Apparatus Suitable for Providing Synchronized Clock Signals to a Microelectronic Device."

Technical Field

The present invention generally relates to microelectronic devices. More particularly, the present invention relates to microelectronic circuits suitable for distributing clock signals.

BACKGROUND OF THE INVENTION

Clock signals are often distributed to portions of a microprocessor to provide synchronization between the various portions of the microprocessor. Microprocessor components such as flip-flops, state machines, and counters rely on such synchronization to step the components through various computations.

A clock signal typically originates at a source that is external to a microprocessor—*e.g.*, at a quartz-crystal circuit on a computer motherboard. The clock signal is transmitted to the microprocessor at one or more points and travels via a clock network on the microprocessor to various clock sinks.

Generally, the clock network is configured to minimize any delay in propagation of the clock signal (clock skew) between various portions of the microprocessor. However, as microprocessors become increasingly integrated, it becomes increasingly more difficult to design the microprocessors with clock trees that minimize clock skew. Accordingly, improved methods and apparatus for reducing clock skew are desired.

SUMMARY OF THE INVENTION

The present invention provides improved apparatus for supplying synchronized clock

signals to portions of an integrated circuit. The way in which the present invention addresses the deficiencies of now-known clock distribution systems is discussed in greater detail below. However, in general, the present invention provides an integrated circuit configured to provide synchronized clock signals to multiple sites on a microprocessor.

In accordance with one exemplary embodiment of the present invention, a clock signal distribution device is formed on a semiconductor substrate. The distribution device is configured to receive a clock signal and distribute synchronized clock signals to multiple locations within the device. In accordance with one aspect of this embodiment, the clock distribution device is formed on a compound semiconductor (*e.g.*, SiGe) substrate to reduce phase noise associated with transmission of the clock signals.

In accordance with a further exemplary embodiment of the present invention, the clock distribution device is configured to couple to a microprocessor and provide synchronized clock signals to multiple locations on the microprocessor. In accordance with one aspect of this embodiment, the distribution device includes conductive bumps configured to facilitate coupling the device to the microprocessor.

BRIEF DESCRIPTION OF THE DRAWING

The drawing figure is a schematic illustration of a clock signal distribution device in accordance with an exemplary embodiment of the present invention;

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

The present invention generally relates to a microelectronic device configured to distribute clock signals. More particularly, the invention relates to an integrated circuit configured to provide synchronized clock signals to various sites. Although this invention may be used to provide synchronized clock signals to a variety of integrated circuits, the invention is conveniently described below in connection with providing the clock signals to a microprocessor.

An exemplary clock signal distribution device 100 in accordance with the present invention is schematically illustrated in the drawing figure. As illustrated, device 100 includes a

clock input 110, clock outputs 120 and 130, clock drivers 140 and 150, transmission lines 160, 170, 180, and 190, and receivers 200 and 210. Although device 100 is illustrated with a single input, two outputs, two drivers, and the like, device 100 may suitably include any number of inputs, outputs, drivers, lines, and the like.

In operation, device 100 receives a clock signal at input 110 and distributes the signal over lines 160 and 170 to drivers 140 and 150, respectively. Clock signals are then transmitted from drivers 140 and 150 over lines 180 and 190 to outputs 120 and 130.

Input 110 is generally configured to receive a clock signal – *e.g.* from a quartz circuit and transmit the signal to drivers 140 and 150. Accordingly, input 110 may be formed of any conductive material such as metal. In accordance with one exemplary embodiment of the invention, input 110 includes a solder bump formed using Controlled Collapse Chip Connection (C4) technology, and a clock input is received by device 100 through one or more conductive bumps.

In accordance with the present invention, drivers 140 and 150 are configured to facilitate clock signal transmission to receivers 200 and 210. Drivers 140 and 150 may include any driver suitable for amplifying a clock signal. In accordance with one exemplary embodiment, drivers 140 and 150 are configured to reduce phase noise associated with typical drivers. One exemplary driver configuration, designed to reduce phase noise, includes forming drivers 140 and 150 using compound semiconductor material such as silicon germanium (SiGe). For example, the drivers may be formed using SiGe substrates using Heterojunction Bipolar Transistor (HBT) technology. Alternatively, the drivers may be formed using a thin film of SiGe or other semiconductor or compound semiconductor material.

Transmission lines 160, 170, 180, and 190 are suitably configured to transmit clock signals between input 110 and outputs 120 and 130. Lines 160-190 may be formed of any conductive material. For example, lines 160-190 my be formed of aluminum, copper, or other conducting material. For example, lines 160-190 may be formed of doped semiconductor material.

Receivers 200 and 210 are configured to receive clock signals from drivers 140 and 150 and transmit the signals to outputs 120 and 130. Receivers 200 and 210 may include any circuit

configured to receive a signal from drivers 140 and 150 and convert the signal for suitable transmission to a portion of the microprocessor. In accordance with an exemplary embodiment, receivers 200 and 210 are formed of SiGe based HBT transistors.

Outputs 120 and 130 are generally configured to receive clock signals from drivers 140 and 150. In accordance with one exemplary embodiment of the present invention outputs 120 and 130 are further configured to electrically couple to portions of a microprocessor. One technique for coupling device 100 to the microprocessor includes use of C4 technology. Thus, in accordance with one exemplary embodiment, outputs 120 and 130 include C4 bumps.

Forming a clock distribution circuit, in accordance with an embodiment of the invention, on a separate substrate may be advantageous for several reasons. For example, clock networks formed on substrates separate from a microprocessor allow for higher clock speeds and less noise associated with the signal because the clock signals are transmitted through fewer active and passive devices, transmission lines can be shielded, microprocessor design can be simplified because clock signal routing does not need to be accounted for, and clock routing scheme layout scan be more readily optimized because microprocessor design criteria can be neglected or mitigated.

As noted above, device 100 is configured to provide synchronic clock signals to outputs 120 and 130. Accordingly, lines 160, 170 and 180, 190 are designed to have the same resistance-capacitance time delay (time delay is generally proportional to resistance*capacity in a line). In accordance with one exemplary embodiment of the invention, lines 180 and 190 are designed to have substantially the same resistance, capacitance, and length. Furthermore, transmission lines 180 and 190 may be configured to cancel noise from signals transmitted from multiple outputs of drivers 140 and 150.

Although the present invention is set forth herein in the context of the appended drawing figure, it should be appreciated that the invention is not limited to the specific form shown. For example, while the invention is conveniently described above in connection with coupling the device to a microprocessor using bump technology, the device may be integral with the microprocessor or integral with one or more devices which are coupled to the microprocessor. Various other modifications, variations, and enhancements in the design and arrangement of the

method and apparatus set forth herein may be made without departing from the spirit and scope of the present invention as set forth in the appended claims.